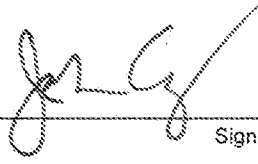
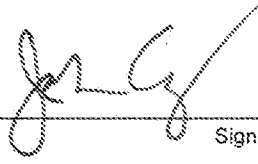
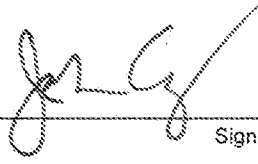


<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional)  2550/185						
<p>I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]</p> <p>on _____</p> <p>Signature _____</p> <p>Typed or printed name <u>John L. Conway</u></p>	<table border="1" style="width: 100%; border-collapse: collapse;"><tr><td style="width: 50%; padding: 5px;">Application Number  10/670,673</td><td style="width: 50%; padding: 5px;">Filed  September 25, 2003</td></tr><tr><td colspan="2" style="padding: 5px;">First Named Inventor  Bruce K. Wachtmann</td></tr><tr><td style="padding: 5px;">Art Unit  2814</td><td style="padding: 5px;">Examiner  Pizarro Crespo, Marcos D.</td></tr></table>		Application Number  10/670,673	Filed  September 25, 2003	First Named Inventor  Bruce K. Wachtmann		Art Unit  2814	Examiner  Pizarro Crespo, Marcos D.
Application Number  10/670,673	Filed  September 25, 2003							
First Named Inventor  Bruce K. Wachtmann								
Art Unit  2814	Examiner  Pizarro Crespo, Marcos D.							
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p>								
<p>I am the</p> <table style="width: 100%;"><tr><td style="width: 50%; vertical-align: top;"><p><input type="checkbox"/> applicant/inventor.</p><p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p><p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>48,241</u></p><p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</p></td><td style="width: 50%; vertical-align: top; text-align: center;"><div style="margin-bottom: 10px;"> _____ Signature <u>John L. Conway</u> _____ Typed or printed name</div><div style="margin-bottom: 10px;"><u>(617) 443-9292</u> _____ Telephone number</div><div><u>10.16.06</u> _____ Date</div></td></tr></table>			<p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>48,241</u></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</p>	<div style="margin-bottom: 10px;"> _____ Signature <u>John L. Conway</u> _____ Typed or printed name</div> <div style="margin-bottom: 10px;"><u>(617) 443-9292</u> _____ Telephone number</div> <div><u>10.16.06</u> _____ Date</div>				
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<p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p>								
<p><input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.</p>								

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wachtmann	Atty. Docket:	2550/185
Serial No.:	10/670,673	Art Unit:	2814
Filing Date:	September 25, 2003	Examiner:	Pizarro Crespo, Marcos D
Invention:	METHOD OF FORMING A SURFACE MICROMACHINED MEMS DEVICE		

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Mail Stop EBC  
Commissioner for Patents  
P.O. Box 1450,  
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Following a Final Office Action dated April 24, 2006 and an Advisory Action dated June 30, 2006, Applicants submit the present Request for Formal Review by a panel of examiners, of the legal and factual basis of the rejections pending in the present case, in accordance with the Pre-Appeal Brief Conference Pilot Program<sup>1</sup>.

Applicants believe that the issue presented is well-posed for appeal, and request formal review prior to appeal on the following grounds:

**I. Background Synopsis of Subject Matter**

In general, MEMS devices may be made by conventional surface micromachining ("SMM") techniques. SMM techniques build material layers on top of a substrate using additive and subtractive processes. Semiconductor junctions formed between a sensor substrate and a conductive path create undesirable parasitic capacitances that can corrupt electrical signals.

In accordance with one aspect of the invention, the subject application discloses a method of forming a surface micromachined MEMS device by applying an oxide insulator to a substrate, and then depositing a conductive path directly on the oxide. The oxide electrically isolates the conductive path from the substrate. The MEMS device illustratively is free of semiconductor junctions formed by the substrate and the conductive path (i.e., the substrate and conductive path do not together form a

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<sup>1</sup> Official Gazette of the United States Patent and Trademark Office, vol. 1296, Number 2, (July 12, 2005).

semiconductor junction). Thus, one source of undesirable parasitic capacitances that can corrupt electrical signals is eliminated.

## II. Synopsis of Status of the Case

Claims 1, 3-5 and 7-20 are pending in the application. Claims 9-14 and 20 stand withdrawn. Claims 1, 3-5, 7, 8, and 15-18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Montague (US 5798283) in view of Kim (US 6500763) and Lee (US 6160314). Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Montague/Kim/Lee in view of Fladre (US 200410152272).

The appeal, noticed concurrently herewith, is with respect to rejected claims, claims 1, 3-5, 7, 8, and 15-19.

## III. Issue for Review Prior to Appeal

**The rejection of claims 1, 3-5, 7, 8, and 15-18 for obviousness rests on Office assertion of a motivation to combine references that lack an evidentiary basis.**

“To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.” Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

The examiner has advanced the knowledge of one skilled in the art as the only motivation to combine the cited references:

“Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art to use either an oxide or a nitride in Montague's method because these were recognized in the semiconductor art for their use as etch/polish stop materials, as taught by Kim and Lee, and **the selection of any of these known equivalents would be within the level of ordinary skill in the art.**” (Office Action of 7/24/06, page 4, para. 1, emphasis added).

However, the Office Action of 7/24/06 provides no evidentiary basis for Examiner's conclusory statement that “**selection of any of these known equivalents would be within the level of ordinary skill in the art.**” At most, the Kim and Lee

references teach that an oxide may be substituted for a nitride for use as an etch/polish stop material under certain narrow conditions. As will be shown below, neither Lee nor Kim teach that an oxide is equivalent to a nitride for all relevant purposes within a semiconductor structure. Absent evidence of such a teaching either in the cited references or in the knowledge of one skilled in the art, a prima facie case of obviousness has not been made.

Claim 1 is directed to a method of forming a surface micromachined MEMS device having both circuitry and structure. Among other things, claim 1 requires “depositing a conductive path directly on an oxide” that was applied to a substrate. This conductive path connects between the circuitry and structure. In contrast, Montague ‘283 teaches depositing polysilicon (a conductive path) on a nitride layer.

Lee ‘314 teaches the use of a complex structure as a polishing stop for fabricating a semiconductor device. This structure is shown in fig. 2A of Lee:

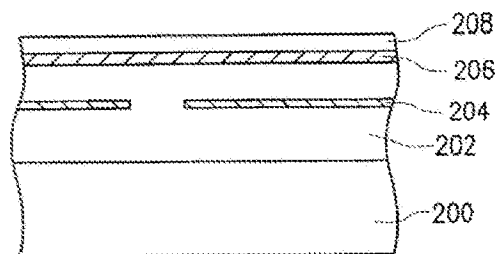


FIG. 2A

Lee describes the structure thusly:

“Referring first to FIG. 2A, a first dielectric layer 202 is formed on a semiconductor substrate 200. The dielectric layer 202, for example, is a silicon dioxide layer. An etching stop layer 204, for example, a silicon nitride layer, is formed in the dielectric layer 202. The materials of the polishing stop layer 206 and the dielectric layer 202 are different. A polishing stop layer 206 is formed on the dielectric layer 202. The material of the polishing stop layer 206 is, for example, silicon-oxy-nitride, silicon nitride or aluminum oxide, which are not easily removed by CMP and have a high polishing selectivity. (See Lee ‘314, col. 2 lines 47 to 62. )

To provide a motivation or a suggestion to replace Montague’s nitride layer

22 with an oxide layer, a reference would need to teach that the materials are fully equivalent in layer 22 in Montague's application or in a similar application. Lee never describes nitride and oxide as interchangeable substitutes when used as a singular insulating layer over a semiconductor substrate. This is the function performed by Montague's layer 22. Instead, Lee mentions that in a layer of the complex sandwich shown in fig. 2A (layer 206), one or more materials would work. Performance as a polishing stop or etch stop is but one attribute of Montague's insulating layer 22.

Kim '763 teaches a method for manufacturing an electrode of a capacitor.

**FIG. 1**

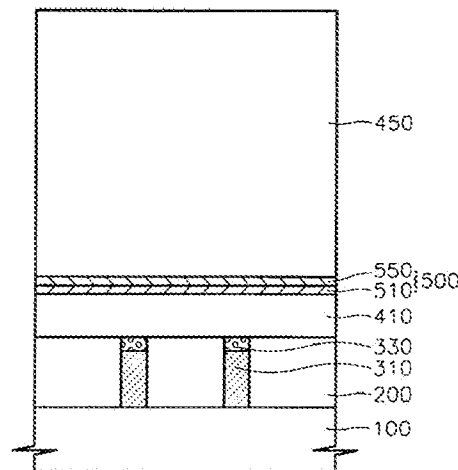


Fig. 1 of Kim '763 shows the structure formed by Kim's process. Kim describes the process, thus:

"In a first embodiment of the present invention, FIG. 1 schematically illustrates a process of forming an etch stop layer 500 and a mold sacrificial insulating layer 450 on a **semiconductor substrate 100**. More specifically, a conductive plug 310, which will be electrically connected to a storage node, is formed on the semiconductor substrate 100 using a standard buried contact process. The conductive plug 310 is surrounded by a lower insulating layer 200 so that the **conductive plug 310** may be insulated from other conductive patterns (not shown) such as gates, which are formed on the semiconductor substrate 100, while the conductive plug 310 is electrically connected to an active region in the semiconductor substrate 100. Put another way, the conductive plug 310 functions as a buried contact. The thickness of the lower insulating layer 200 varies with necessity, but may be about 4000-5000 ÅNG. depending on the thickness of the conductive plug 310. ... Thereafter, the **etch stop layer 500**, which will be used in a later etching process, is formed on the support insulating layer 410. In one embodiment of the present invention, the etch stop layer 500 includes a tantalum oxide layer 510.... (See Kim '763, col. 3, line 31 to col. 4, line 11.)

Thus, in Kim '763, conductor 310 lies between substrate 100 and the etch stop layer 500. While Kim may teach that in Kim's specific complex semiconductor structure, the etch stop layer may be an oxide, one of skill in this art could not infer from this teaching that Montague's insulating layer 22 can be either a nitride or an oxide. Montague's insulating layer 22 lies between the conductive path and the substrate and serves additional functions as compared to Kim's etch stop layer 500. Equivalence of materials can only be inferred from consideration of all relevant properties of the materials. Kim '763 like Lee '314 cannot serve as motivation or a suggestion to replace Montague's insulating layer with an "all oxide" layer since there is no teaching in Kim that the oxide would perform equally well or better than the nitride in Montague's device structure. Thus, claim 1 is deemed non-obvious over Montague in view of Kim '763.

Since claim 1 is allowable over the cited art, claims 3-5, 7 and 8, which depend from claim 1 and add further limitations are also allowable for at least the same reasons as for claim 1. Claim 15 and dependent claims 16-18 are also allowable for the same reasons as for claim 1.

Because the conclusory statement cited above that the Examiner relies on to show motivation to combine references, without supporting evidence, must be found insufficient as a matter of law, the examiner has not borne the examiner's burden of coming forward with a prima facie case of obviousness. Allowance of claims 1 and 15, and all claims dependent therefrom, is respectfully requested. *See, Zurko*, 258 F.3d 1739, 1786 (Fed. Cir., 2001).

Respectfully submitted,



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Attorney for Applicants

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